

Low-Power and High Speed High-to-Low Level Shifter

Vazgen Sh. Melikyan, Ani L. Aleksanyan, Vache A. Galstyan, Sergey H. Manukyan, Ani S. Harutyunyan and Sandra Ilijin

Abstract—A novel structure of high speed high-to-low level shifter is proposed. Due to decrease in the number of input thick-oxide transistors, the output frequency maximum is increased while providing 13.5% less power consumption than conventional designs. The utilization of dual thick-oxide NMOS input cascade provides smaller output signal jitter and approximately 50% duty-cycle. The circuit is designed in CMOS 40nm technology and simulated with SPICE.

Index Terms—level shifter, low-power, high-speed, power dissipation, multicore, CMOS, thick-oxide transistor.

I. INTRODUCTION

THE emergence of portable devices requires novel power management techniques which will assure overall low-power and high speed performance. Various power reduction methodologies are currently known.

One of most widely used techniques is supply voltage scaling for separate IC blocks. Supply voltage reduction will cause a decrease of overall power consumption of current structure in the expense of its performance. [1-2]. Moreover, in modern system on chips (SoCs) different functional units are manufactured on a single die, which require different supply voltages to obtain desirable performance of each block [3].

To provide connection between blocks which process multi-voltage signals, level shifters are used which have simple function to convert the signal from one voltage level to another.

Another use of level shifters is the data signal connection between core circuits and I/O circuitry. Hence, they can have dual functionality to provide both high-to-low and low-to-high conversion. To provide overall low-power performance of the system, level shifters have to be optimized to consume lowest possible power [5].

Power consumption in CMOS circuits consists of two different components: dynamic and static. Dynamic power dissipation (1) is mainly caused by charging and discharging the load capacitance [4].

$$P_{dyn} = C * f * VDD^2 \quad (1)$$

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The static power dissipation is due to the leakage current of reverse biased pn junction diode of MOSFET structure (2).

$$P_{stat} = I_{leak} * VDD \quad (2)$$

Power consumption can be reduced by scaling supply voltage and capacitance. As supply voltage is scaled down, the problems of leakage current, deficient noise margins and small voltage swings arise. Because of the process technology is scaled, the leakage power has become important component of overall power consumption [6], [7].

The proposed level shifter in comparison with conventional design demonstrates lower power consumption, smaller occupied area. as well as smaller output delay.

The paper is arranged in the following order. Section II describes the structure of conventional design of level shifter. Section III demonstrates the principles and main characteristics of proposed solution. Section IV presents the SPICE simulation results and comparison of both structures. Section V brings the conclusion.

II. THE DESIGN AND CHARACTERISTICS OF CONVENTIONAL LEVEL SHIFTER

The structure of conventional level shifter, which is shown in Fig. 1, uses the cascaded inverters. The first inverter is the input cascade of the level shifter and it is connected between the high supply voltage (VDDH) and ground. For that reason, thick-oxide transistors (MN1, MP1) are used to withstand the high voltage input. The circuit operates as follows: when the input is at logical low or equal 0 V, MN1 is turned “off” and the MP1 is turned “on”. Therefore the output node of the first cascade is charged up to voltage level of VDDH.

High voltage output of first stage is then transferred to second inverter which also uses thick-oxide transistors, but in this case, is connected to low supply voltage (VDD). This means that the output signal dynamic range of second stage coincides with VDD, which itself is transferred to the third stage of thin-oxide inverter. In design, the 2.5 V and 1.2 V supply voltage levels are used for VDDH and VDD respectively.

The characteristics of this design (Fig.1) are shown in Table I for different environmental conditions.

The disadvantage of this structure is big amount shoot-through current flowing from VDD/VDDH to ground in the case when both PMOS and NMOS transistors are open. Also, the state transition current significantly increases the power consumption of the design. The big number of used thick-

oxide transistors leads to slower switching of input stages, thus increasing the time when PMOS/NMOS input transistors are simultaneously open, which yields to additional power consumption.

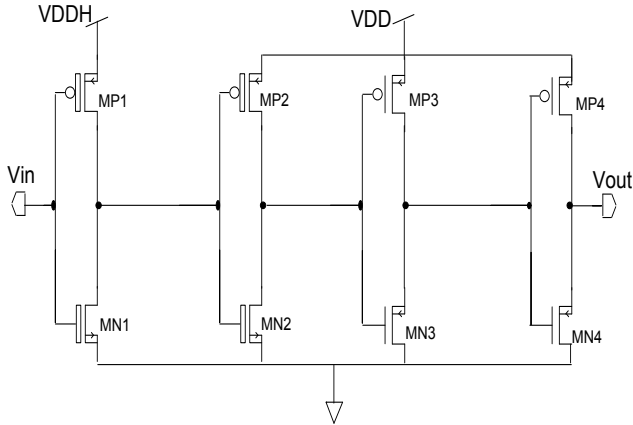


Fig. 1. The conventional Level Shifter with thin-oxide transistors.

TABLE I
CHARACTERISTICS OF CONVENTIONAL UP-DOWN LEVEL SHIFTER FOR DIFFERENT ENVIRONMENTAL CONDITIONS

Parameter/Symbol	Min	Typ.	Max	Unit
Freq. f	1000	1000	1000	MHz
Low Supply voltage (VDD)	1.08	1.2	1.32	V
High supply voltage (VDDH)	2.38	2.5	2.62	V
I_{avg}	38.9	39.1	39.2	μ A
I_{max}	24.56	25.34	26.85	mA
P_{max}	29.62	30.41	31.75	mW
Temperature (T)	-40	25	125	$^{\circ}$ C

Besides, the transistor sizes of the second cascade (MP2, MN2) should be large enough to drive the following stages. As channel width of PMOS transistor should be approximately three times larger than of NMOS, it leads to the unacceptable increase of occupied area.

In case when signals at the input for second stage have high frequencies and high voltage levels, the output signal level which drives the third stage with thin-oxide input transistors, can exceed the low supply voltage level, thus being potential threat to those transistors. To solve this problem thin-oxide third stage transistors (MP3, MN3) are replaced by thick-oxide ones preventing the unacceptable high levels of input signal. This solution is widely used in current level shifters; however it leads to greater area and power consumption, because the total number of thick-oxide transistors is increased.

III. THE DESIGN AND CHARACTERISTICS OF PROPOSED LEVEL SHIFTER

The proposed design of level shifter, which is shown in Fig.2, uses fewer transistors to achieve similar output results. Besides, the proposed design uses dual NMOS input cascade to drive the output thin-oxide PMOS transistor. This eliminates the shoot-through current of the stage thus lowering the overall power consumption of the design.

Another advantage of this solution is that maximal switching frequency of NMOS transistor is higher than of PMOS as it is generally known that $\mu_n > \mu_p$. Moreover, the elimination of one thick-oxide PMOS transistor saves additional area, thus lowering the occupied area of the design.

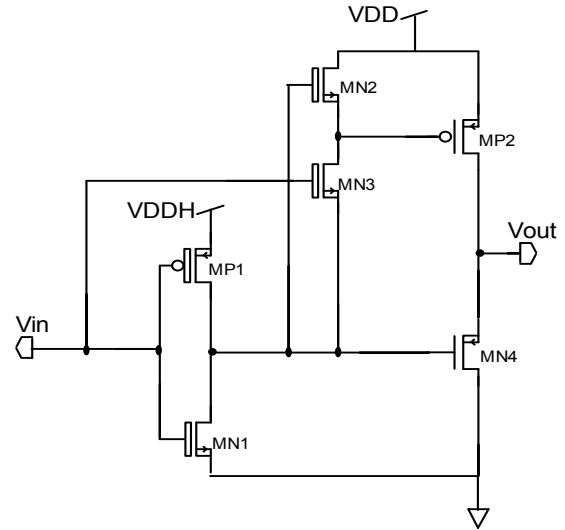


Fig. 2. The structure of proposed level shifter

Because the dual NMOS structure has low supply voltage, and the output signal level maximum must be by V_{th} less than the source voltage, there is no hazard for thin-oxide PMOS transistor to undergo unacceptably high input voltage impact.

TABLE II
CHARACTERISTICS OF PROPOSED UP-DOWN LEVEL SHIFTER FOR DIFFERENT ENVIRONMENTAL CONDITIONS

Parameter/Symbol	Min	Typ.	Max	Unit
Freq. f	1000	1000	1000	MHz
Low Supply voltage (VDD)	1.08	1.2	1.32	V
High supply voltage (VDDH)	2.38	2.5	2.62	V
I_{avg}	30.8	31.1	32.5	μ A
I_{max}	20.86	21.73	22.95	mA
P_{max}	25.07	26.08	27.09	mW
Temp. (T)	-40	25	125	$^{\circ}$ C

However, this structure has one major disadvantage. that is the requirement for VDDH and VDD voltage difference to be less than the threshold voltage of transistors MN2 and MN3 to assure the possibility for transistor's turning ON.

The characteristics of proposed design (Fig.2) are shown in

Table II for different environmental conditions.

IV. SIMULATION RESULTS AND ANALYSIS

The proposed and conventional level shifters are implemented in 40 nm CMOS technology and they are optimized to occupy comparable on-chip area. The level shifters are simulated by SPICE simulator, using three process corners (FF, TT, SS processes with respective voltage and temperature values) [8]. Simulations are performed for 1000 MHz input signal frequency, the amplitude swing of 2.5 V and the output level swing of 1.2 V.

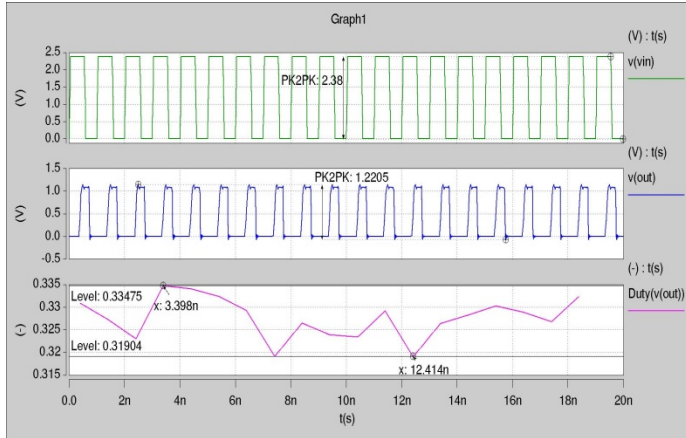


Fig. 3. Output waveform of the conventional level shifter for SS corner

The Fig.3 shows the input and output waveforms of conventional high-to-low level shifter. The input voltage is equal to 2.38 V (the waveform is for SS PVT corner) and output voltage is 1.2205 V respectively. It can be seen from the waveform that duty cycle of the output signal is in range from 31% to 33%.

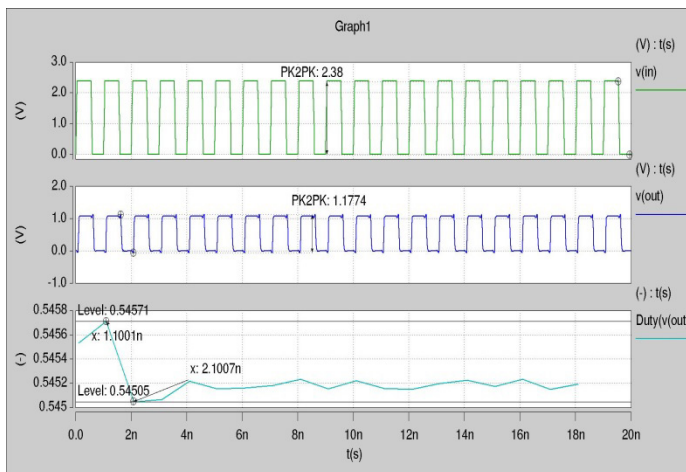


Fig. 4. Output waveform of the proposed level shifter for SS corner

The Fig.4 shows the input and output waveforms of proposed high-to-low level shifter. The input voltage is equal to 2.38 V (waveform is for SS PVT corner) and output voltage is 1.1774 V respectively. In this waveform, the duty cycle of the output signal is about 54.5%.

As the comparative analysis shows, the duty cycle of proposed design is more acceptable than the corresponding result of conventional level shifter.

The period jitter of conventional level shifter is shown in Fig. 5. The simulation is run for three PVT corners (TT 25°C, SS 125°C, FF -40°C) and a peak-to-peak jitter of 36.076 ps is obtained. The maximum and minimum values of period jitter are 18.413 ps and -17.663 ps respectively.

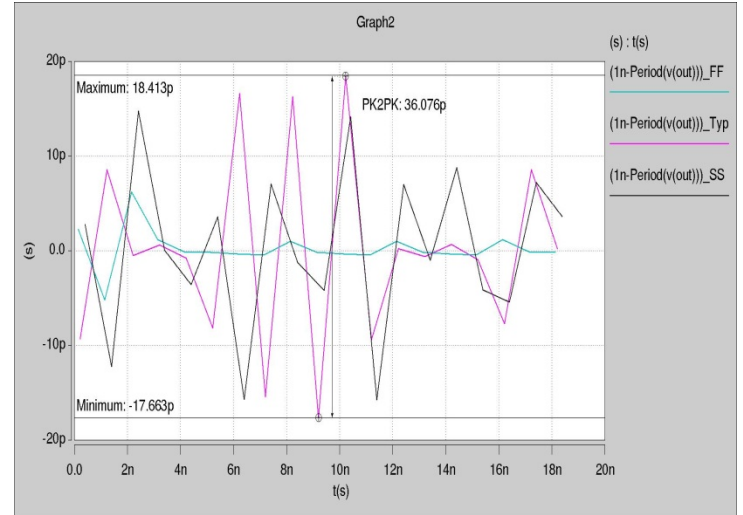


Fig. 5. Period jitter of the conventional level shifter for three PVT corners (TT, FF, SS)

The period jitter of proposed level shifter is shown in Fig. 6. The simulation is run for three PVT corners (TT 25°C, SS 125°C, FF -40°C) and a peak-to-peak jitter of 0.89 ps is obtained. The maximum and minimum values of period jitter are 0.29 ps and -0.59 ps respectively.

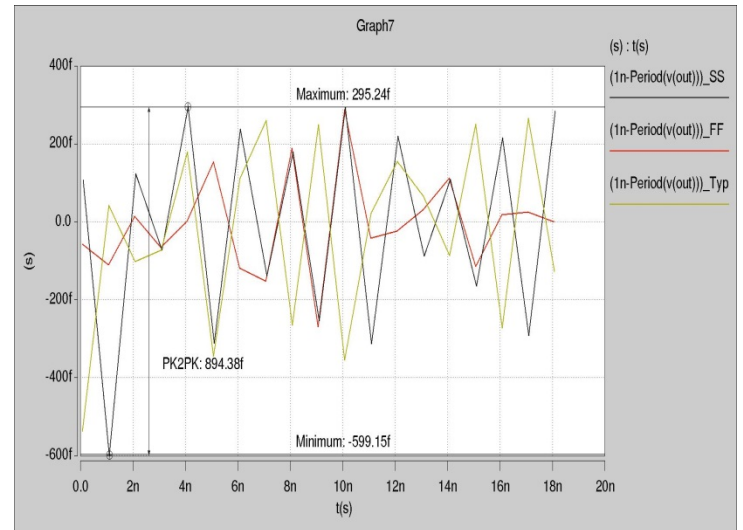


Fig. 6. Period jitter of the proposed level shifter for three PVT corners (TT, FF, SS)

V. CONCLUSION

A novel low-power high-speed level shifter is presented. Due to decrease of number of thick-oxide input components, the proposed design shows better performance in the context of maximum output signal frequency and duty-cycle. The simulation results show that the peak-to-peak period jitter of the proposed design is 0.89 ps and duty cycle is approximately 54.5%. The proposed design decreases the number of thick-gate transistors, thus increasing permissible frequency range and keeping the occupied area small. Also, the design provides 13.5% savings in power consumption compared with conventional design, which makes it a good choice in low-power systems.

ACKNOWLEDGMENT

This work was supported by State Committee Science MES RA, in frame of the research project № SCS 13-21130.

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